Amendments to claims 1-4 recite "[a]n integrated circuit for liquid crystal display...", which are made for clarification purposes. This amendment does not incorporate new matter. Accordingly, Applicants respectfully request entry of the amendments.

Applicants' undersigned representative would like to thank the Examiner for the Interview on June 12, 2002. As outlined by the Interview Summary sheet, an agreement was reached whereby "[i]t was agreed that the Otani reference may not teach the delay circuit as claimed." The Examiner further states that she "will review the Otani reference and [per]form an update search if necessary upon receiving the after-final amendment." Applicants request that the present action be removed from final. Applicants' remarks below memorialize the position set forth in the Interview.

The Office Action states that the arguments presented in the last response with respect to claim 1-18 have been considered but are moot in view of the new grounds of rejection. The Office Action rejects claims 1-18 over Shimamoto (which was referenced in the last Office Action) in view of Otani (U.S. Patent No. 4,967,413). The Office Action reiterates the reasoning for relying on the Shimamoto reference, but recognizes that Shimamoto fails to specifically teach that the transfer is performed with an intermittent time lag. The Office Action relies on Otani to teach the usage of a delay circuit (215) in a channel quality detector to reduce noise and other erroneous data. The Office Action states that it would have been obvious to reduce the transfer time of the display data to the display drivers, which would prevent the loss of data and also the probability that other erroneous data is mistakeningly handled. Applicants respectfully traverse this rejection.

Applicants submit that the features of the present invention as embodied by the claims are neither taught nor suggested by the Shimamoto reference and that there is insufficient motivation to combine the teachings of Otani into Shimamoto.

Shimamoto concerns conversion of serial data to parallel data to accommodate transfer of a large number of bits for high-resolution display. That is, in the Shimamoto display, signals are transferred serially at a low voltage and high speed from a display controller to a flat panel. A low voltage serial data parallel conversion circuit restores the low voltage signals, which are supplied to a flat panel driving/controlling circuit. Therefore, by reducing the signal level, display signal interface lines can be reduced as well as reducing EMI. While Shimamoto is concerned with reduction of electromagnetic wave noise, the foregoing different solution is applied to achieve it. As acknowledged by the Office Action, Shimamoto fails to disclose or suggest reducing the number of simultaneous changes of display data output signals to lower the occurrence of EMI.

Otani, as referenced by the Office Action, relates to an apparatus for detecting quality of signals used in satellite communication systems. In the rejection, the Office Action references col. 5, line 55-col. 6, line 24, for showing a delay circuit to reduce noise and other erroneous data. The delay circuit of Otani is incorporated into a channel quality protector 202 that prevents delivering even a no-error signal that falls below a predetermined quality level thereby reducing noise and other erroneous data.

Applicants have reproduced below certain features of the independent claims 1, 5, 9, and 13 of this application that are neither disclosed nor suggested by Shimamoto, Otani, or the combination thereof.

> Claim 1 recites, *inter alia*, "points of changing said data output signals with respect to a time base are set with time delays that lag one

another during one period of a reference internal clock signal, so that number of simultaneous changes of display data output signals is reduced."

Claim 5 recites, *inter alia*, "points of changing said display data output signals with respect to a time base are set with time delays that lag one another during one period of a clock output signal or a reference internal clock signal having a same phase as the clock output signal, so that number of simultaneous changes of display data output signals is reduced."

Claim 9 recites, *inter alia*, "red, green and blue colored display data composed of plural bits are transferred ... each transfer is performed with a time delay that lags incrementally for each bit unit formed of plural bits optionally selected from each of said display data."

Claim 13 recites, *inter alia*, "a display timing control circuit for transferring red, green and blue color display data formed of plural bits to the TFT drive circuit...; and a delay unit provided in the displayed timing control circuit to delay the transfer timing between one bit unit and another."

EMI is typically caused by simultaneously changing each data output signal of a multi-port system, which causes a high momentary generated current. This current creates electromagnetic noise, which negatively affects other system components. As embodied by claims 1, 4, 9, and 13, this problem is overcome by time delay data output from one another, as embodied by the claims above. Therefore, only a small current is generated by each change thereby reducing the negative affects of EMI on other system components. Common to independent claims 1, 4, 9, and 13, this time delay feature is claimed, which is neither disclosed nor suggested by the Shimamoto reference and as acknowledged by the Office Action.

The Office Action opines that it would have been obvious to use the delay circuit of Otani to accommodate the time delay feature as recited by the claims. However, Otani teaches the use of a delay circuit for employing integration, not in the manner as claimed.

Referring to Fig. 7 of Otani, operation of the burst signal detection apparatus will now be discussed. The circuitry of Fig. 7 is configured to detect channel quality. Maximum Metric Detector 211 and Minimum Metric Detector 210 detect the maximum one and minimum one, respectively, of the metrics of all states in the Viterbi decoder 201. These values are fed to the subtractor 212, the difference being delivered to the adder 213. In order to perform integration, a "delay circuit" 215 must be utilized. The time setter 216 sets the time delay and applies the same to the delay circuit 215, which affects the accuracy of integration. Once delayed, the integrated result of the closed loop is fed to the comparator 214, which compares the integration result with a predetermined value. In this way, channel quality may be detected.

The delay circuit 215 delays bits output from the adder 213 for the purposes of integration and eventual comparison with a predetermined value to detect channel quality. Therefore, only signals of a certain quality are outputted, and signals of this quality have a lower occurrence of error. This delay circuit 215 does not operate in the manner as recited by the claims. That is, the delay circuit 215 does not affect the timing of the output signals with respect to one another, as suggested. As recited by the reproduced claims above, output signals are delayed with one another, so as to overcome EMI problems. As taught by Otani, the delay circuit 215 in combination with the comparator 214 and other components reduce error by employing an integration and comparison routine.

Applicants submit that Otani fails to provide any motivation to affect the delay of the "data output signals" (claim 1), the "display data output signals" (claim 5), and the "red, green and blue colored display data composed of plural bits" (claim 9), such that the

time delay of respective output signals lag one another during a respective clock period (claims 1 & 5) or the delay lags incrementally for each bit unit...(claim 9). Nor is there any motivation to accommodate "a display timing control circuit for transferring red, green and blue color display data formed of plural bits to the TFT drive circuit...; and a delay unit provided in the displayed timing control circuit to delay the transfer timing between one bit unit and another" (claim 13).

Even if the delay circuit 215 was combined with the teachings of Shimamoto, the structure as recited above in the reproduced claims could not be accomplished. The delay circuit 215 of Otani is employed for integration purposes, not for delaying respective output signals or display signals or transfer timing from one bit to another.

As the Office Action acknowledges that Shimamoto fails to disclose or suggest "that the transfer is performed with a time lag little by little for each bit unit formed of plural bits optionally selected from each of the color display data", and in view of the deficiencies of both Shimamoto and Otani, Applicants submit that the obviousness rejection of claims 1, 5, 9, and 13 and respective dependents is improper.

Applicants reproduce below certain features of independent claim 14 that are neither disclosed nor suggested by Shimamoto, Otani, or the combination thereof.

> Claim 14 recites, inter alia, "a detector circuit for detecting a coincidence of polarity by comparing a polarity of bit for each predetermined group of image data outputted by the data display circuit; a first control circuit ...; and a second control circuit for outputting data ... when the coincidence of polarity of bit has been detected by the detector circuit."

The Office Action references columns 6-7, lines 56-26, respectively, citing the first and second control circuit of claim 14. The cited portion of Shimamoto relates to the

arrangement of the parallel/serial (P-S) converter. There is no disclosure or suggestion of operation with respect to a coincidence of polarity. In particular, there is no disclosure or suggestion of a detector circuit for detecting a coincidence of polarity by comparing a polarity of bit for each predetermined group of image data outputted by the data supply circuit, as claim 14 recites. Nor is there a suggestion of a first and second control circuit for outputting data...when the coincidence of polarity of bit has been detected by the detector circuit, as claim also recites. Applicants have thoroughly reviewed the Otani reference and fail to find any disclosure or suggestion of the aforementioned features of claim 14. For these reasons, Applicants submit that the obviousness rejection of claim 14 and respective dependents is improper. Withdrawal of the rejection is respectfully solicited.

Conclusion

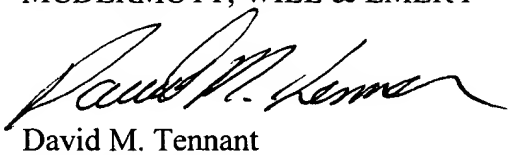
As Shimamoto and Otani, alone or in combination, fail to disclose or suggest each and every feature of claims 1, 5, 9, 13, and 14; and there is no motivation to combine; the applied obviousness rejection is not appropriate. Claims dependent therefrom are patentable at least due to their dependency and for the reasons stated above. Withdrawal of the rejection is respectfully solicited.

In light of the foregoing remarks, the outstanding rejection has been overcome. Applicants respectfully solicit allowance of this case.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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APPENDIX SHOWING CHANGES MADE

IN THE CLAIMS:

Claims 1-4 were amended as follows:

1. (Twice Amended) An integrated circuit for liquid crystal display characterized in that multi-port data output signals are generated with respect to a data input signal, and points of changing said data output signals with respect to a time base are set with time delays that lag one another during one period of a reference internal clock signal, so that number of simultaneous changes of display data output signals is reduced.

2. (Amended) An integrated circuit for liquid crystal display according to claim 1, wherein the points of changing the data output signals with respect to the time base are set to points respectively delayed from an active edge of the clock output signal by 0.5 period, 1 period, and 1.5 period of the data input signal.

3. (Twice Amended) An integrated circuit for liquid crystal display according to claim 1, wherein the points of changing the data output signals with respect to the time base are set to points respectively having time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the data input signal.

4. (Twice Amended) An integrated circuit for liquid crystal display according to claim 1, wherein the points of changing the data output signals with respect to the time base are set to points respectively having time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half

period of the data input signal and by a delay time produced by a delay circuit added to the optional integer times as long as a half period of the data input signal.